

INTRODUCTION

The CCD60 is part of the new L3Vision[®] range of products from e2v technologies. This device uses a novel output amplifier circuit that is capable of operating at an equivalent output noise of a few electrons at frame rates of 1 kHz.

The sensor is a frame transfer device, designed for high frame rate applications such as wavefront sensing or adaptive optics. The device operates in inverted mode to suppress dark current. No antiblooming is supplied, for maximum sensitivity.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by a low noise output amplifier.

The on-chip gain in the charge domain can be adjusted by control of the multiplication phase operating voltage $R\phi 2HV$.

GENERAL DATA

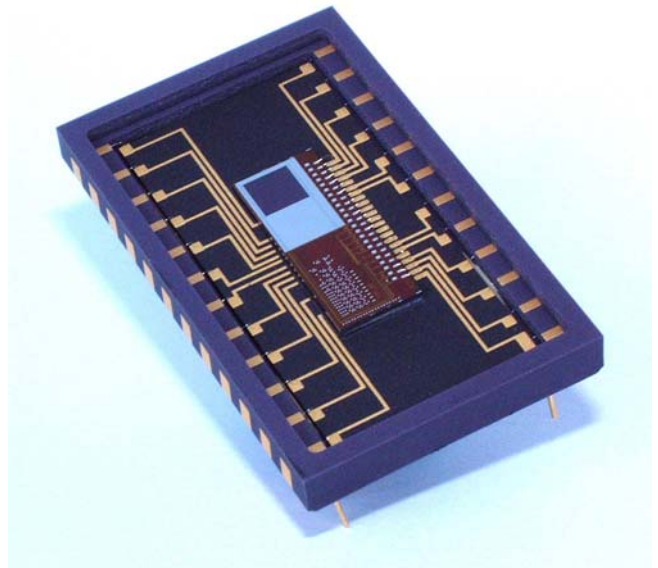
Active image area	3.072 x 3.072 mm
Image section active pixels	128 (H) x 128 (V)
Image pixel size	24 x 24 μ m
Number of output amplifiers	1
Fill factor	100%
Spectral range	400 - 1060 nm

PACKAGE DETAILS (Nominal, see Fig. 11)

Ceramic Package 24-pin DIL

Overall dimensions	32.89 x 20.07 mm
Number of pins	24
Inter-pin spacing	2.54 \pm 0.15 mm
Opposite row spacing	15.24 \pm 0.25 mm
Window material	quartz or removable glass
Mounting position	any

Pin 1 is identified by a spot on the upper package face.



STORAGE AND OPERATION TEMPERATURE EXTREMES

	MIN	MAX
Storage temperature (°C)	-200	+100
Operating temperature (°C)	-120	+75
Temperature ramping (°C/min)	-	5

Note: Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

TYPICAL PERFORMANCE SPECIFICATIONS

The following are for operation of front-face devices at 500 Hz frame rate and at typical operating voltages. Parameters are given at 293 K unless specified otherwise. Where parameters are different in the normal and high gain mode, both are given.

PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity (normal mode) (see note 1)	$\mu\text{V}/\text{e}^-$	-	1.3	-
Multiplication register gain (see notes 2 and 3)		1	-	1000
Peak signal - non-inverted mode operation (see note 1)	e^-/pixel	-	600k	-
Peak signal - inverted mode operation	e^-/pixel	-	200k	-
Charge handling capacity of gain register (see note 4)	e^-/pixel	-	800k	-
Readout noise at 11 MHz (normal mode) (see note 5)	$\text{e}^- \text{ rms}$	-	100	-
Readout noise at 11 MHz (high gain mode) (see note 5)	$\text{e}^- \text{ rms}$	-	< 1	-
Dark signal at 293 K (see note 6)	$\text{e}^-/\text{pixel}/\text{s}$	-	1100	-
Dark signal non-uniformity (DSNU) at 293 K (see notes 6 and 7)	$\text{e}^-/\text{pixel}/\text{s}$	-	500	-
Excess noise factor (see note 8)		1	-	1.4
Maximum readout frequency (settling to 1%) (see notes 1 and 9)	MHz	-	11	18
Maximum parallel transfer frequency	MHz	-	10	-

NOTES

1. These values are predicted from design and not measured.
2. The typical variation of gain with $R\phi 2\text{HV}$ is shown in Fig. 1.
3. Some increase of $R\phi 2\text{HV}$ may be required throughout life to maintain gain performance. Adjustment up to the maximum level specified under the Operating Conditions is possible.
4. When gain is employed, a linear response of output signal with input signal is achieved for output signals up to typically 400 ke^- .
5. These noise values are dominated by reset noise in the output amplifier and it is assumed that correlated double sampling (CDS) is not being employed. If CDS is used to suppress the reset component, a noise of 10 e^- can typically be achieved at a pixel rate of 1 MHz with a noise floor of $4 \text{ e}^- \text{ rms}$. At 11 MHz the noise with CDS is about 35 e^- . These values are inferred by design and not measured.
6. The dark signal has the usual temperature dependent component and an additional weakly temperature dependent component, which is independent of the integration time.
7. DSNU is defined as the 1σ variation of the dark signal.
8. The excess noise factor is defined as the input referred noise with gain divided by the input referred noise without gain.
9. A maximum readout frequency of 18 MHz is expected to be achievable with a 20 pF load and single sampling.

ORDERING INFORMATION

PART NUMBER	OPERATING MODE	ANTI-BLOOMING	WINDOW
CCD60-01-* -B42	IMO	None	Temporary

DEVICE COSMETIC PERFORMANCE

Grade 1 devices are supplied to the blemish specification shown below.

Note that incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

Test Conditions

Operating mode	Device run in standard 2-phase mode at a rate of 500 frames/second.
Sensor temperature	22 ± 3 °C.
Multiplication gain	Set to approximately 1000.
Illumination	Set to give a signal level of approximately $50 e^-$ /pixel/frame.

BLEMISH SPECIFICATION

Black Columns Black defects are counted when they have a responsivity of less than 90% of the local mean signal at approximately the specified multiplication gain and level of illumination. A black column contains at least 9 contiguous black defects.

White Columns White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5% of multiplication register capacity at a gain of 1000. A white column contains at least 9 contiguous white defects.

Pin-Head Columns Pin-head columns are manifest as a partial dark column with a bright pixel showing photoresponse at the end of the column furthest from the readout register. Pin-head columns are counted when the black column has a responsivity of less than 90% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

SPECIFICATION FOR GRADE 1 DEVICES

PARAMETER	SPECIFICATION
White Columns	0
Black Columns	0
Pin-head Columns	0

Figure 1: TYPICAL VARIATION OF GAIN WITH $R\phi 2HV$ AT $T = 20\text{ }^\circ\text{C}$

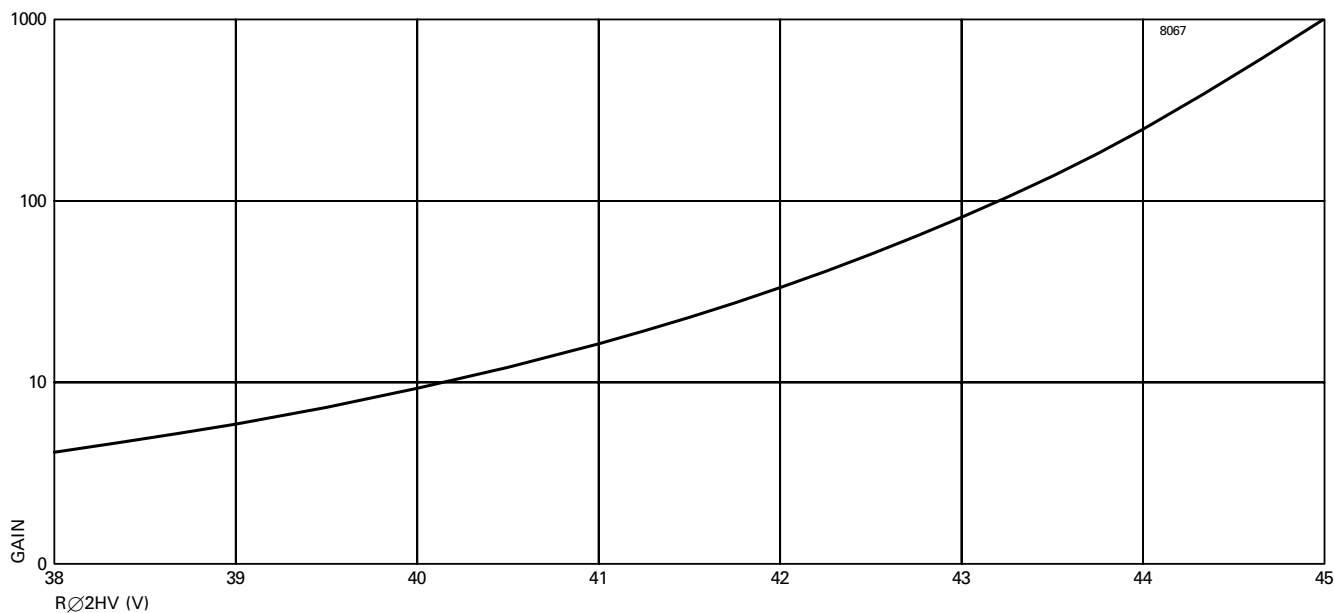
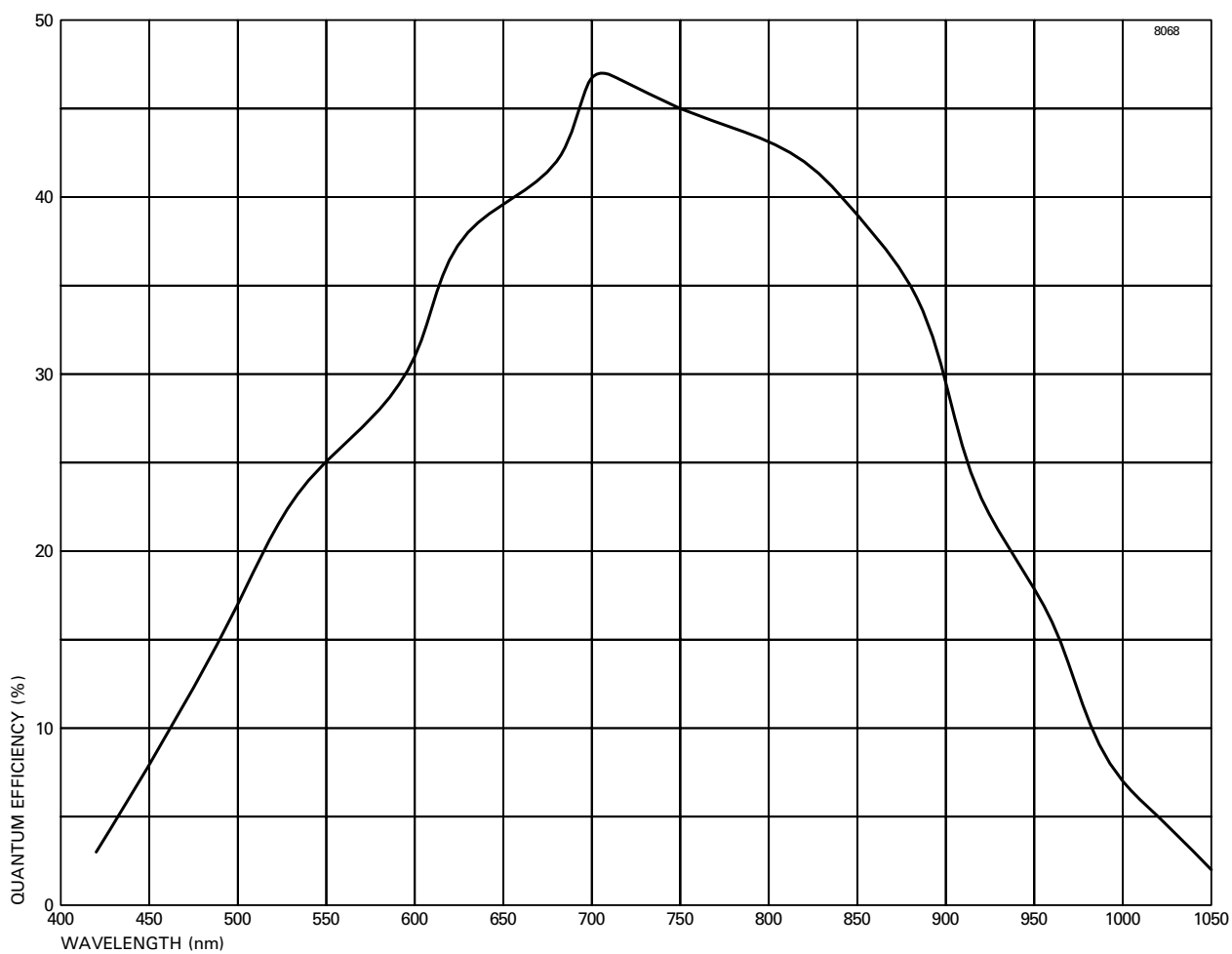


Figure 2: TYPICAL SPECTRAL RESPONSE OF FRONT-ILLUMINATED DEVICE



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to SS.

PIN	CONNECTION	MIN (V)	MAX (V)
1	RØ2HV	-20	+50
2	RØDC	0	+10
3	OD	-0.3	+32
4*	OS	-0.3	+25
5	SS	0	
6	ØR	-20	+20
7	SS	0	
8	IØ1	-20	+20
9	IG	-20	+20
10	ABD	-0.3	+25
11	SØ1	-20	+20
12	SØ2	-20	+20
13	IØ2	-20	+20
14	SØ1	-20	+20
15	SØ2	-20	+20
16	DG	-20	+20
17	RØ2	-20	+20
18	RØ1	-20	+20
19	RØ3	-20	+20
20	RØ1	-20	+20
21	RØ2	-20	+20
22	OG	-20	+20
23	RD	-0.3	+25
24	RØDC	-20	+20

* Permanent damage may result if, in operation, OS experiences short circuit conditions.

Maximum voltages between pairs of pins:

PIN	CONNECTION	PIN	CONNECTION	MIN (V)	MAX (V)
3	OD	4	OS	-15	+15
1	RØ2HV	2	RØDC	-20	+50
1	RØ2HV	24	RØDC	-20	+50
1	RØ2HV	19	RØ3	-20	+50
Output transistor current (mA)					20

ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

CONNECTION	PULSE AMPLITUDE OR DC LEVEL (V)		
	Min	Typical	Max
I \emptyset 1,2 high	+4 (see note 10)	+5	+7 (see note 10)
I \emptyset 1,2 low	-	-5	-
S \emptyset 1,2 high	+4 (see note 10)	+5	+7 (see note 10)
S \emptyset 1,2 low	-	-5	-
R \emptyset 1,2,3 high	+10	+12	+13
R \emptyset 1,2,3 low	-	0	-
R \emptyset 2HV high	+20	+40	+50 (see note 3)
R \emptyset 2HV low	0	+4	+5
\emptyset R high	+10 (see note 11)	+12	+13 (see note 11)
\emptyset R low	-	0	-
R \emptyset DC	+2	+3	+5
OG	+1	+3	+5
SS	0	+4.5	+7
OD	+25	+28	+32
RD	+15	+18	+20
ABD	+20	+24	+25
IG	-	-5	-
DG low	-	0	-
DG high	+10	+12	+13

NOTES

10. I \emptyset and S \emptyset adjustment may be common.

11. \emptyset R high level may be adjusted in common with R \emptyset 1,2,3.

An external load is required. This can either be a resistor of about 2.2 k Ω (non-critical) or a constant current type of about 7.5 mA. The total on-chip power dissipation at 500 Hz frame rate is approximately 200 - 250 mW, depending on the details of the voltages and clock timings used.

DRIVE PULSE WAVEFORM SPECIFICATION

The following are suggested pulse rise and fall times for operation at 500 Hz frame rate, and with pixel readout at 11 MHz. The device has a 2-phase construction, so timing and overlaps are not critical for the I \emptyset and S \emptyset clocks.

CLOCK PULSE	TYPICAL RISE TIME (ns)	TYPICAL FALL TIME (ns)	TYPICAL PULSE OVERLAP
I \emptyset	20	20	@90% points
S \emptyset	20	20	@90% points
R \emptyset 1	5	5	@90% points
R \emptyset 2	5	5	@90% points
R \emptyset 3	5	5	@90% points
R \emptyset 2HV	Sine	Sine	Sinusoid- high on falling edge of R \emptyset 1

NOTES

- Register clock pulses are as shown in the line timing diagram.
- An example clocking scheme is shown in the line timing diagram. R \emptyset 2HV can also be operated with a normal clock pulse, as shown in the frame timing diagram. The requirement for successful clocking is that R \emptyset 2HV reaches its maximum amplitude before R \emptyset 1 goes low.

ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS				
Connection	Capacitance to SS	Inter-phase Capacitances	Total Capacitance	Units
I \emptyset 1 (see note 14)	750	100	850	pF
I \emptyset 2 (see note 14)	750	100	850	pF
S \emptyset 1 (see note 14)	750	100	850	pF
S \emptyset 2 (see note 14)	750	100	850	pF
R \emptyset 1	36	41	77	pF
R \emptyset 2	56	41	97	pF
R \emptyset 3	62	60	122	pF
R \emptyset 2HV	45	49	94	pF
SERIES RESISTANCES				
Connection	Approximate Total Series Resistance			
I \emptyset 1	9			Ω
I \emptyset 2	9			Ω
S \emptyset 1	9			Ω
S \emptyset 2	9			Ω
R \emptyset 1	7			Ω
R \emptyset 2	7			Ω
R \emptyset 3	7			Ω
R \emptyset 2HV	8			Ω
AMPLIFIER				
Output Impedance	250			Ω

NOTE

- For operation in the inverted mode. For operation in the non-inverted mode, the capacitance to substrate is 400 pF and the total capacitance is 500 pF.

Figure 3: CLOCKING SCHEME FOR MULTIPLICATION GAIN
(Sine wave clocks)

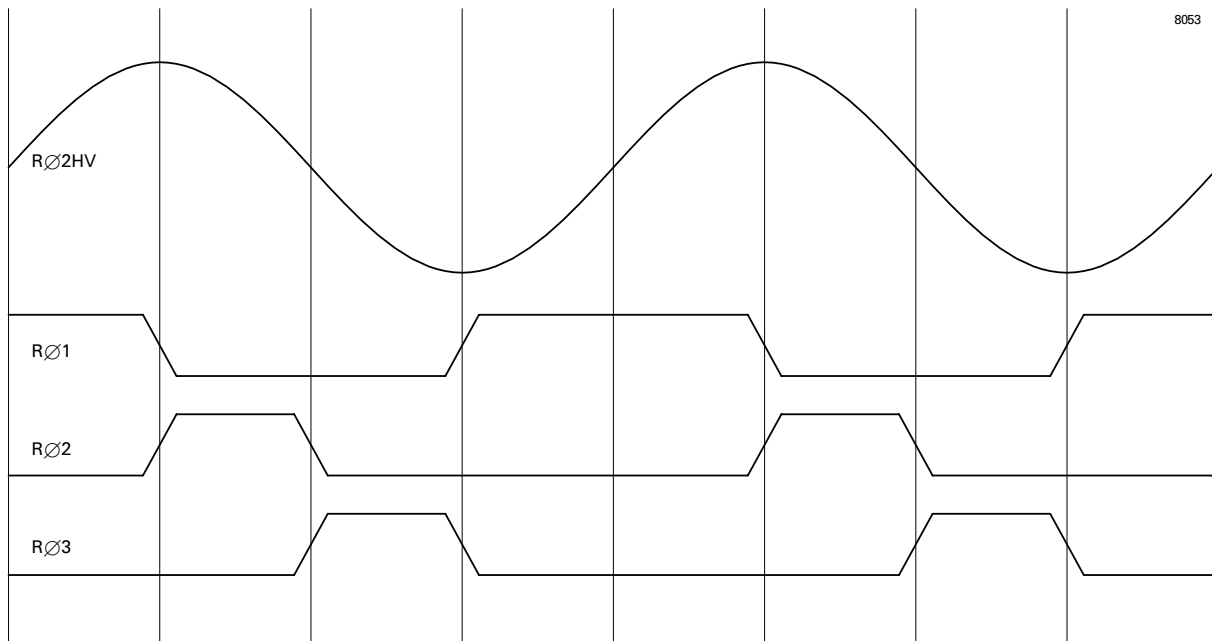
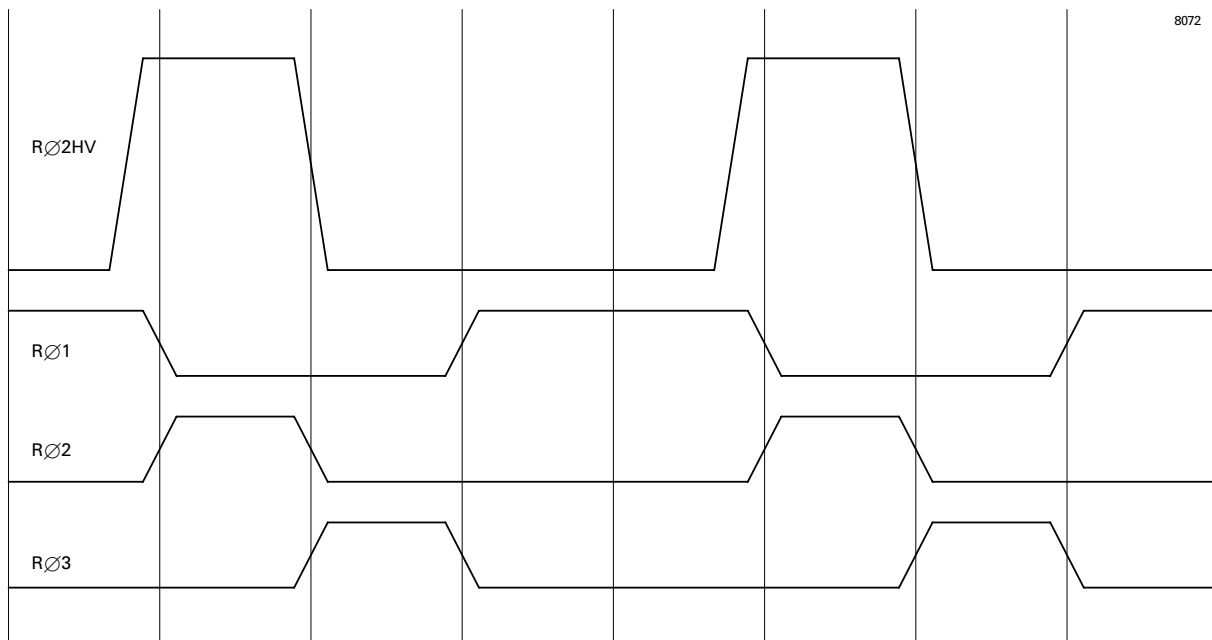
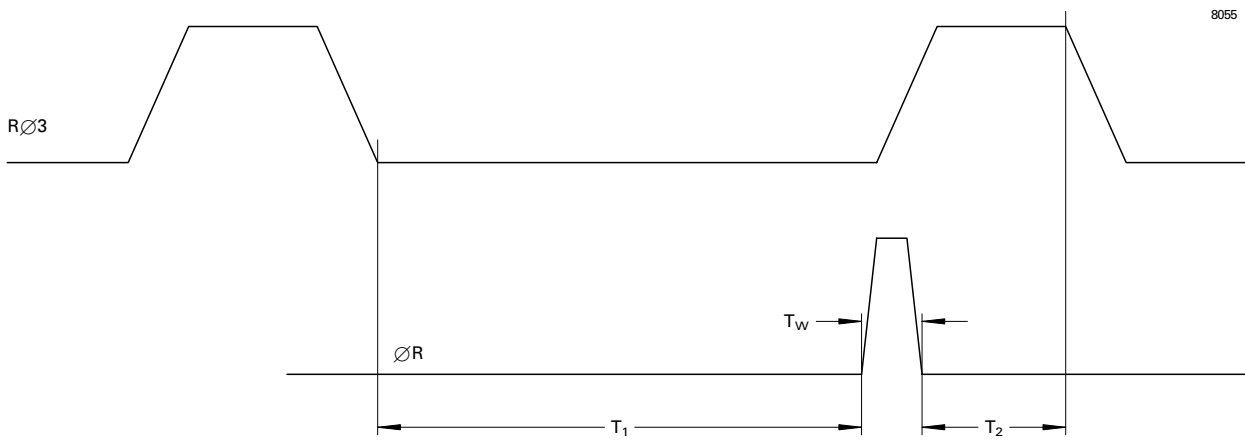


Figure 4: CLOCKING SCHEME FOR MULTIPLICATION GAIN
(Normal clock pulses)



PULSE TIMINGS AND OVERLAPS

Figure 5: RESET PULSE



$T_w = 10$ ns typical
 $T_1 =$ output valid
 $T_2 > 0$ ns

Figure 6: PULSE AND OUTPUT TIMING

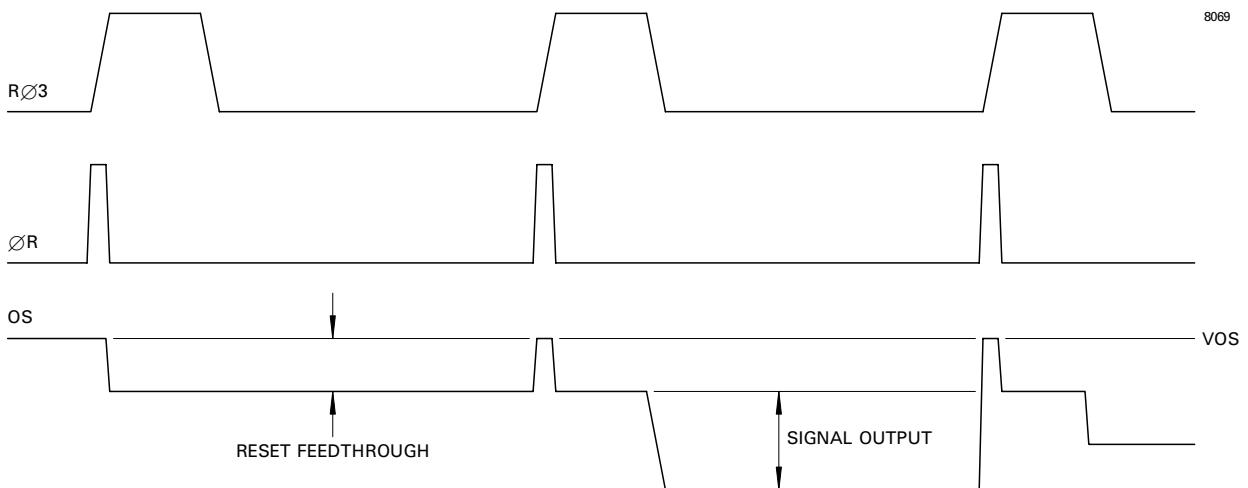


Figure 7: LINE TIMING DIAGRAM

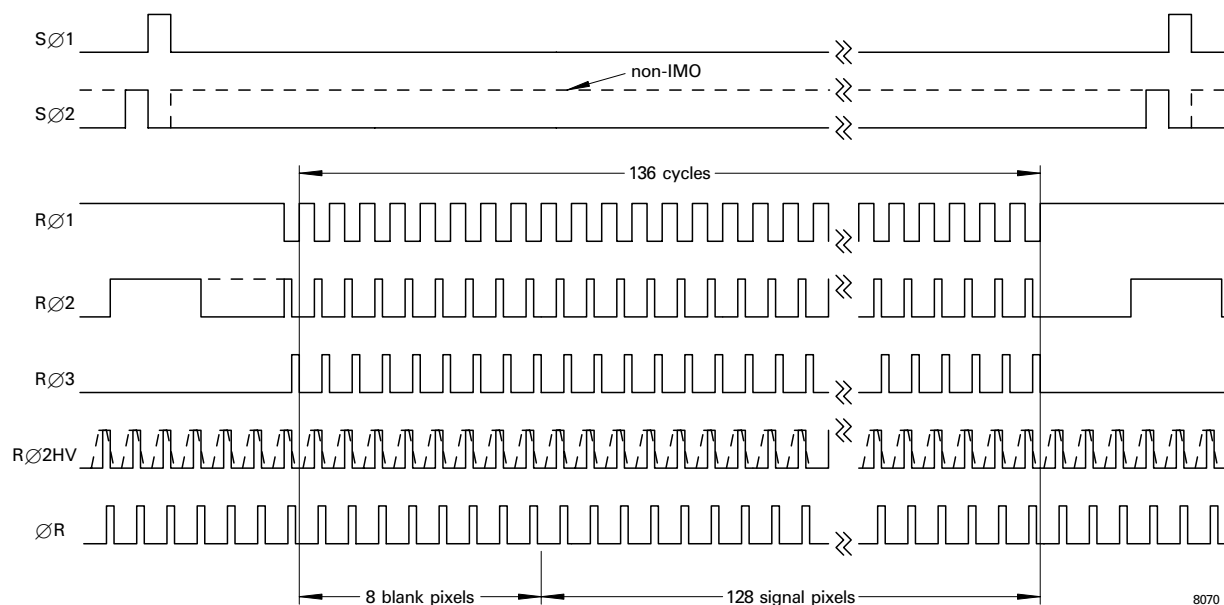


Figure 8: FRAME TIMING DIAGRAM

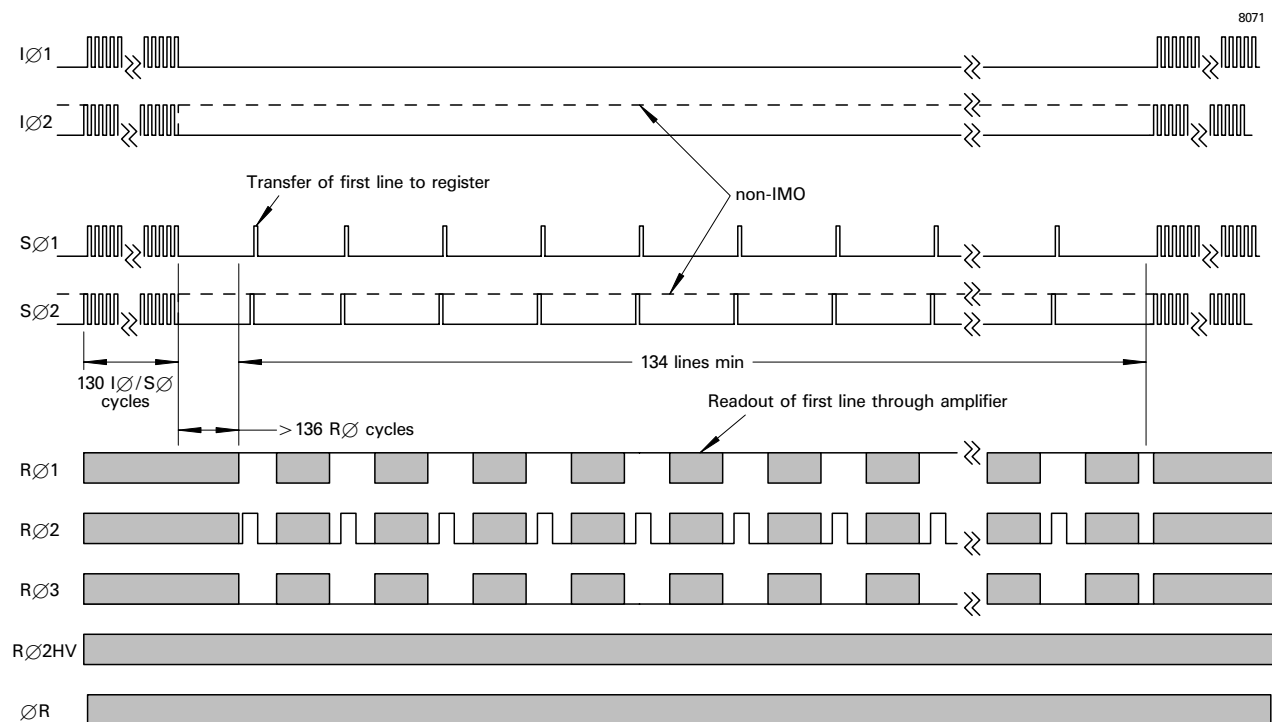


Figure 9: SCHEMATIC CHIP DIAGRAM

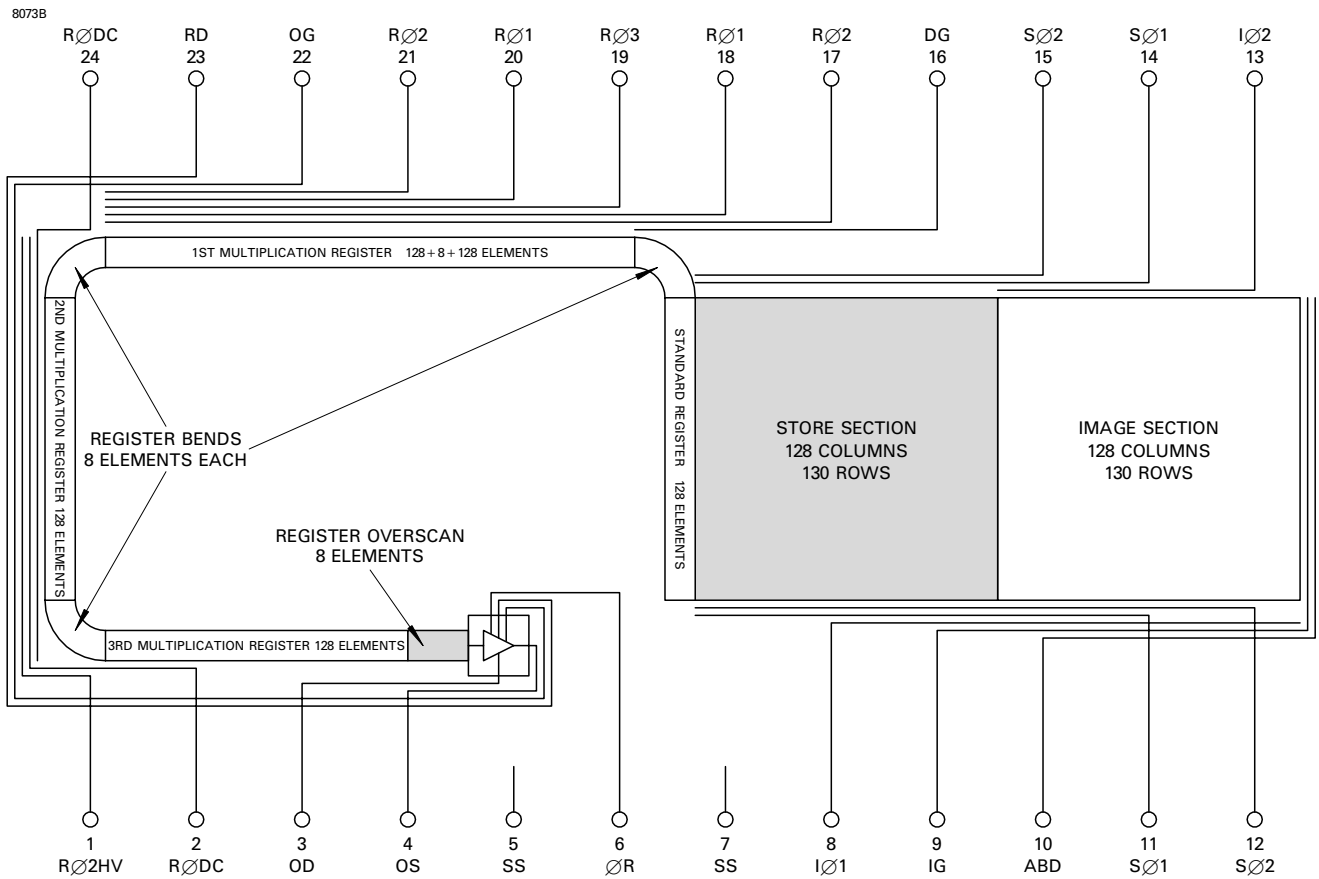


Figure 10: OUTPUT CIRCUIT SCHEMATIC

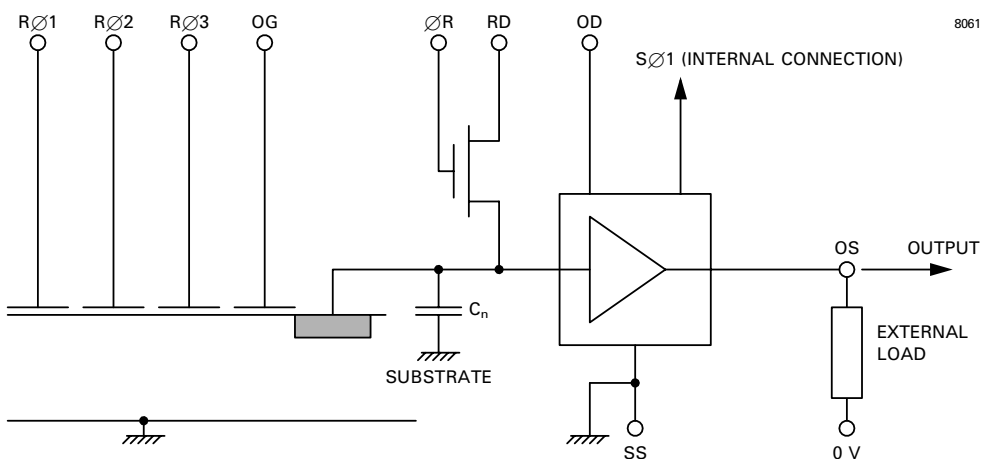
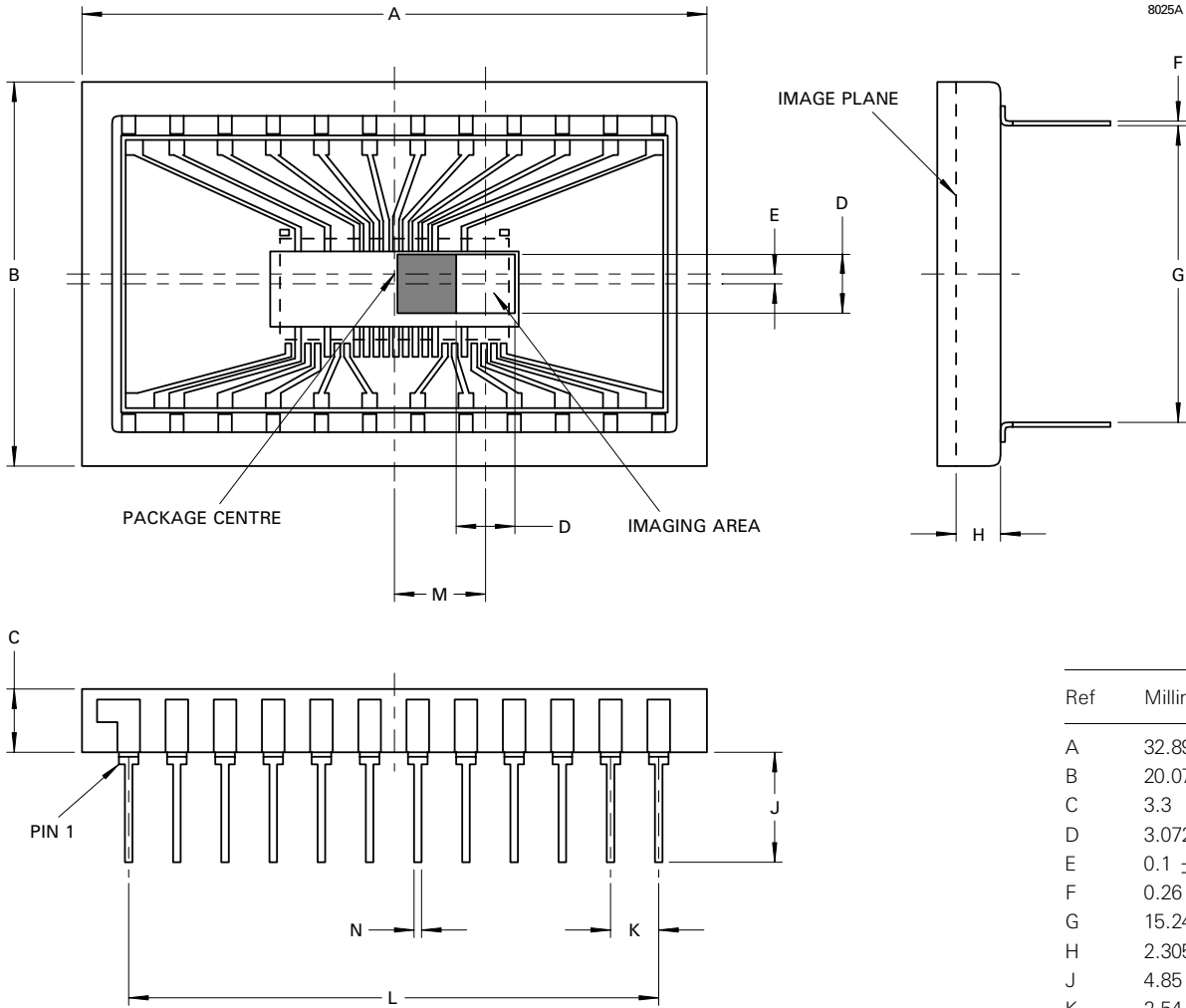


Figure 11: PACKAGE OUTLINE
 (All dimensions without limits are nominal)



Ref	Millimetres
A	32.89
B	20.07
C	3.3
D	3.072
E	0.1 ± 0.5
F	0.26 ± 0.04
G	15.24 ± 0.25
H	2.305 ± 0.600
J	4.85 min
K	2.54 ± 0.15
L	27.94 ± 0.15
M	4.76 ± 0.50
N	0.46 ± 0.20

Outline Note

The image centre position shown is provisional for engineering samples. Contact e2v technologies to confirm the position as it may be adjusted in future.

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